Fig_1

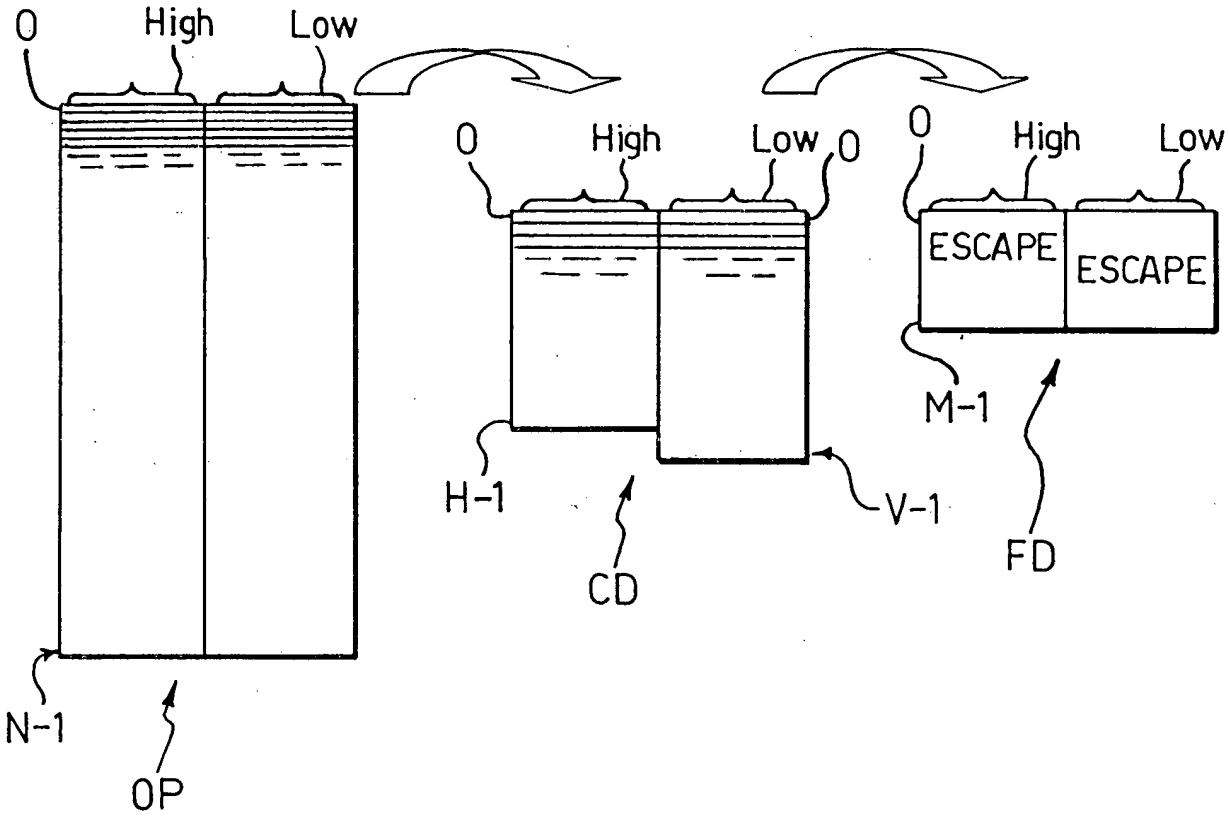
0
High
Low
N-1
OP
0
High
Low
0
H-1
CD
V-1
0
High
Low
ESCAPE
ESCAPE
M-1
FD

Fig_2

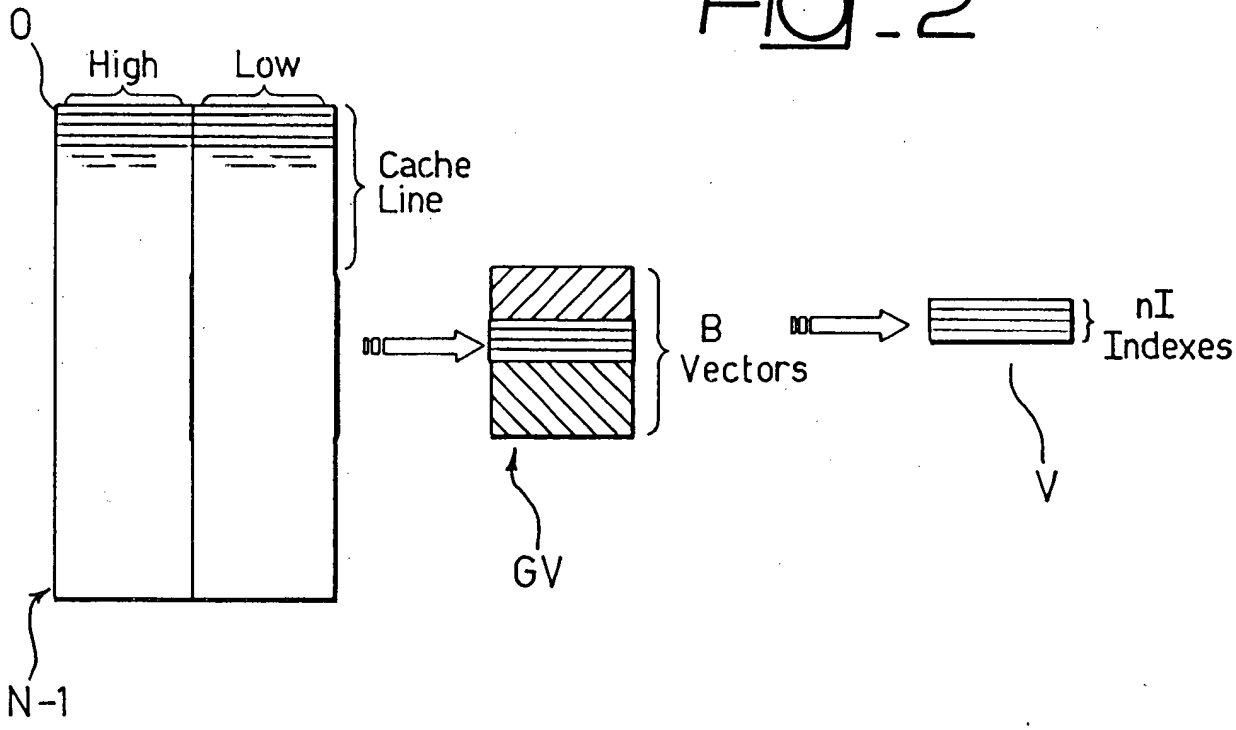
0
High
Low
Cache Line
N-1
B Vectors
GV
nI Indexes
V

Fig_3

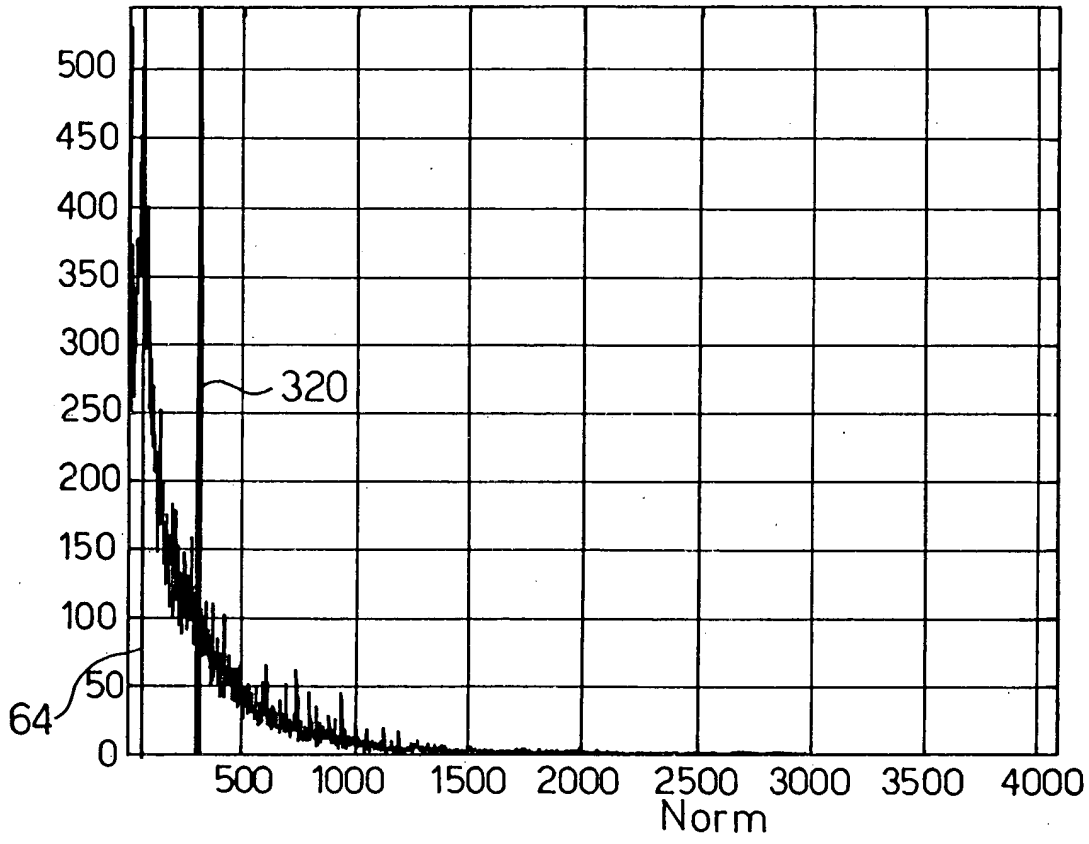
500
450
400
350
300
250
200
150
100
50
0
320
64
500
1000
1500
2000
2500
3000
3500
4000
Norm

Fig_4

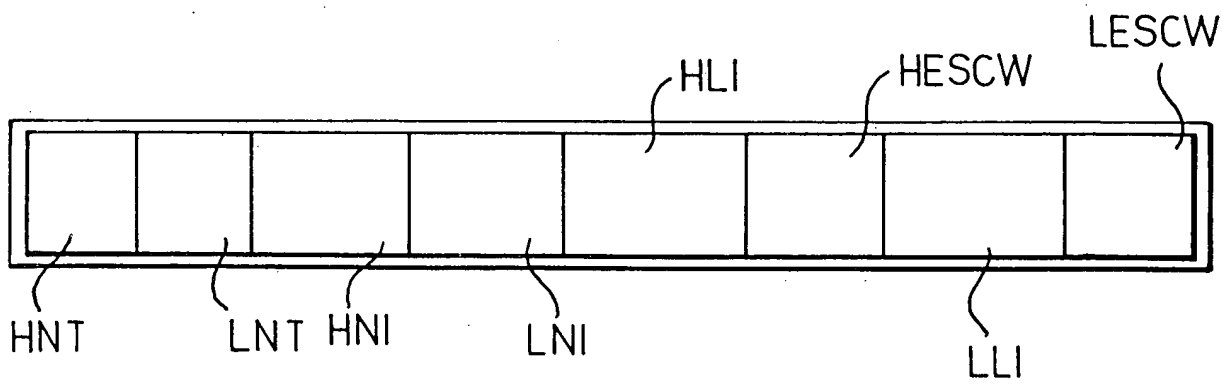
LESCW
HLI
HESCW
HNT
LNT
HNI
LNI
LLI

Fig_5

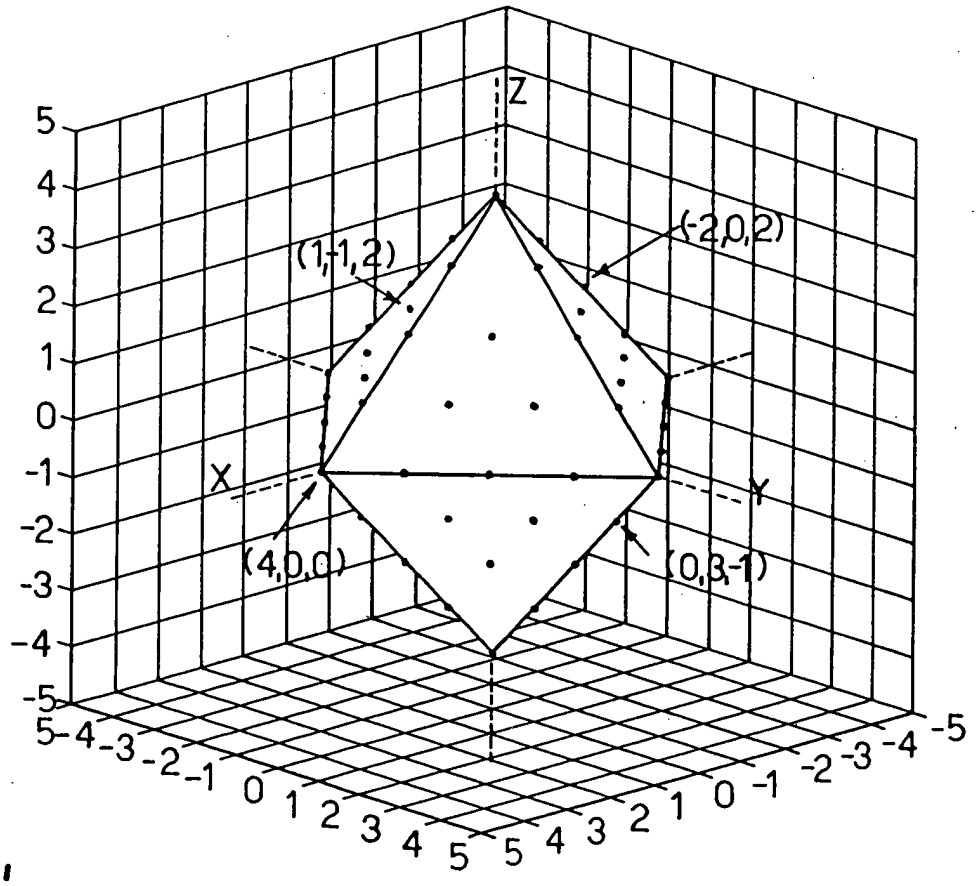

Fig_8

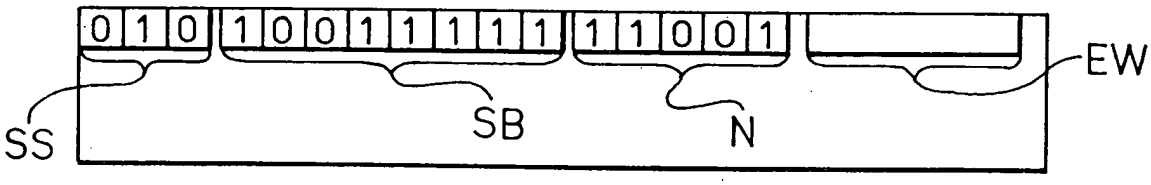

Fig_9

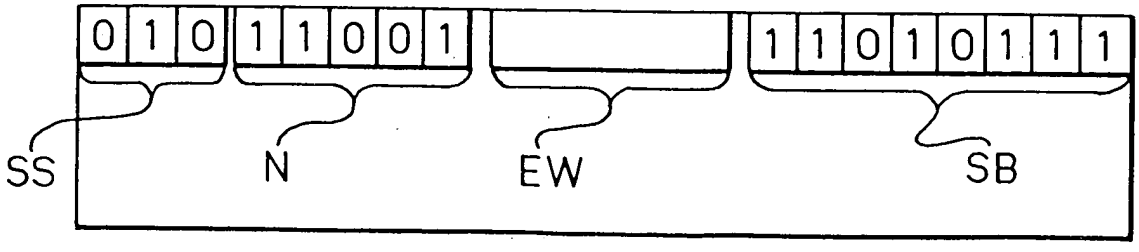

Fig_6

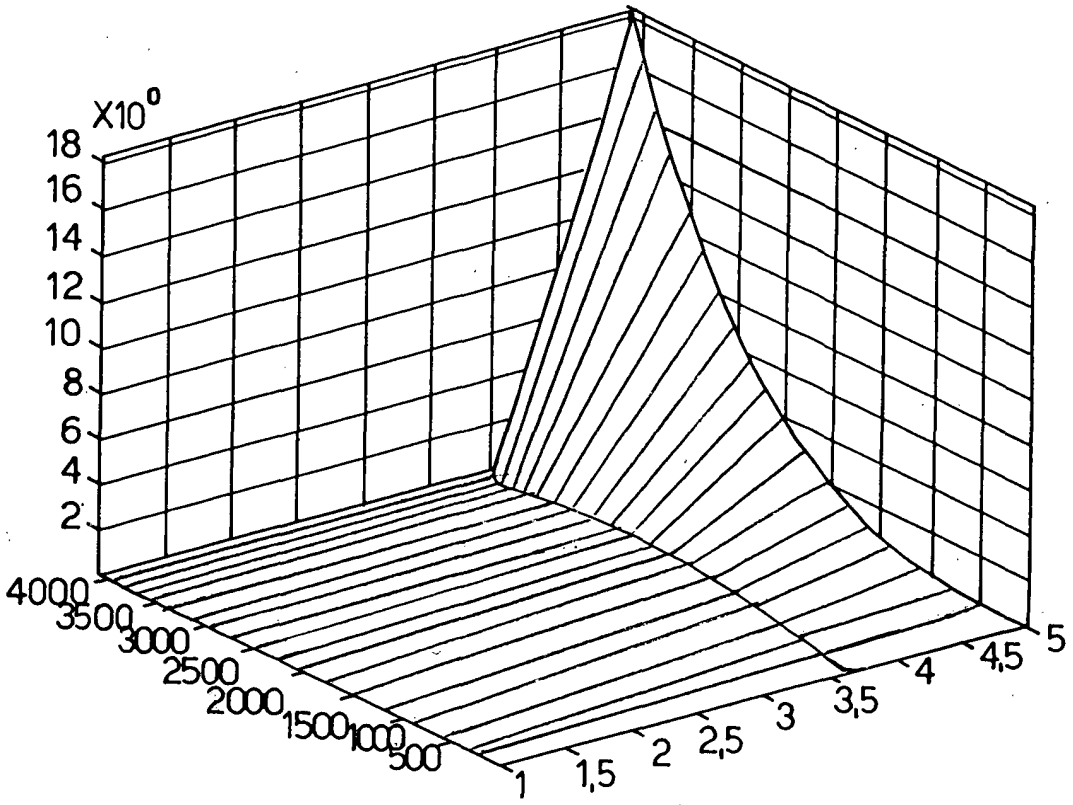
X10^0
18
16
14
12
10
8
6
4
2
4000
3500
3000
2500
2000
1500
1000
500
1
1,5
2
2,5
3
3,5
4
4,5
5

Fig_7

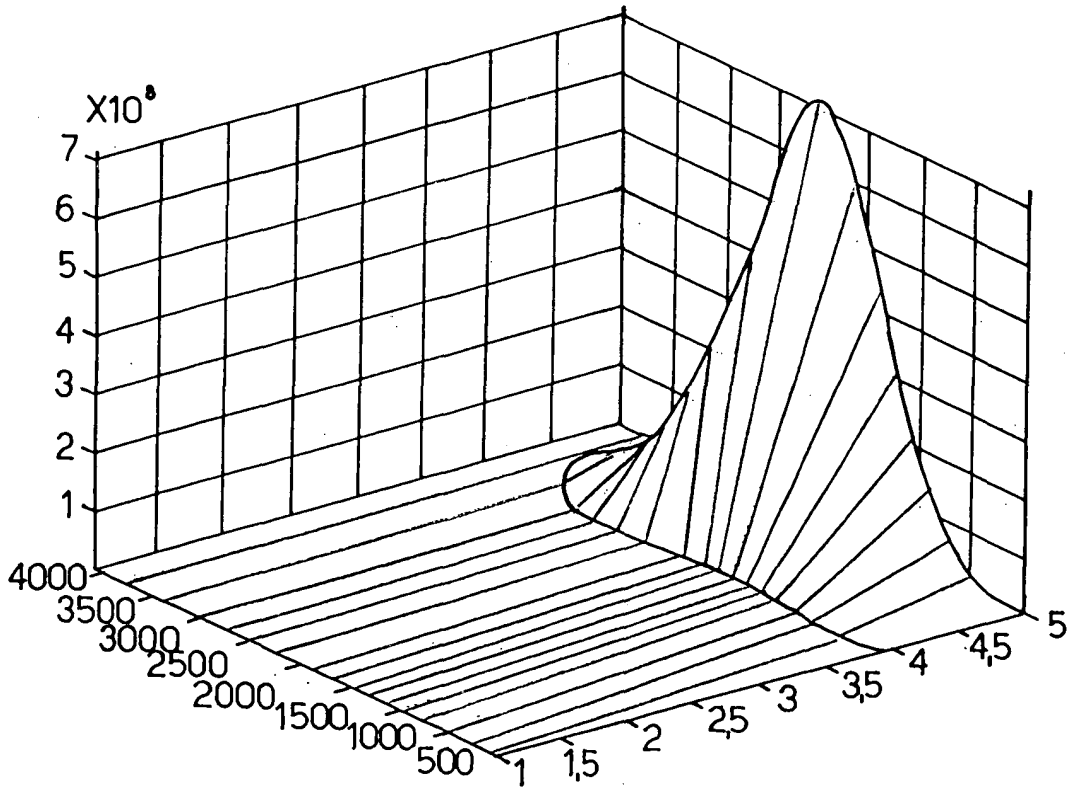
X10^8
7
6
5
4
3
2
1
4000
3500
3000
2500
2000
1500
1000
500
1
1,5
2
2,5
3
3,5
4
4,5
5

Fig_10

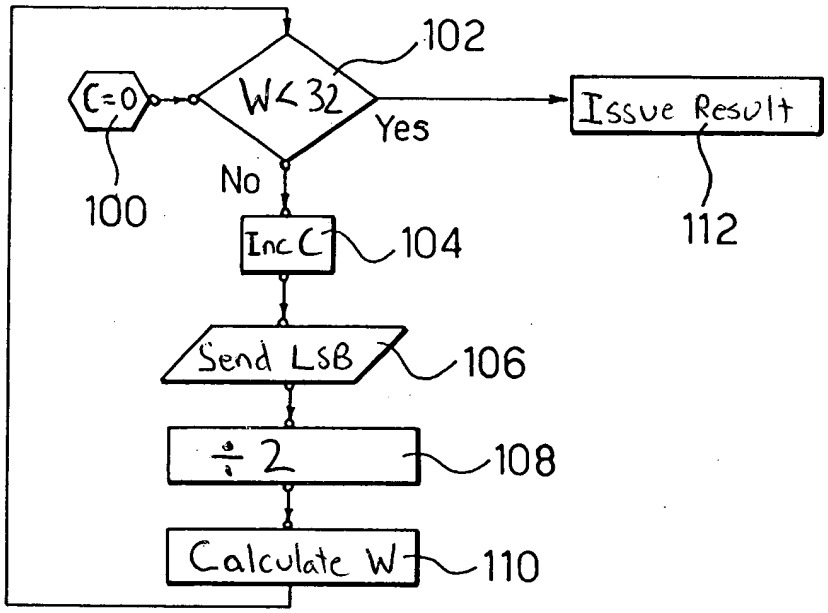
C=0
W<32
Yes
No
Issue Result
Inc C
Send LSB
÷ 2
Calculate W
100
102
104
106
108
110
112

Fig_11

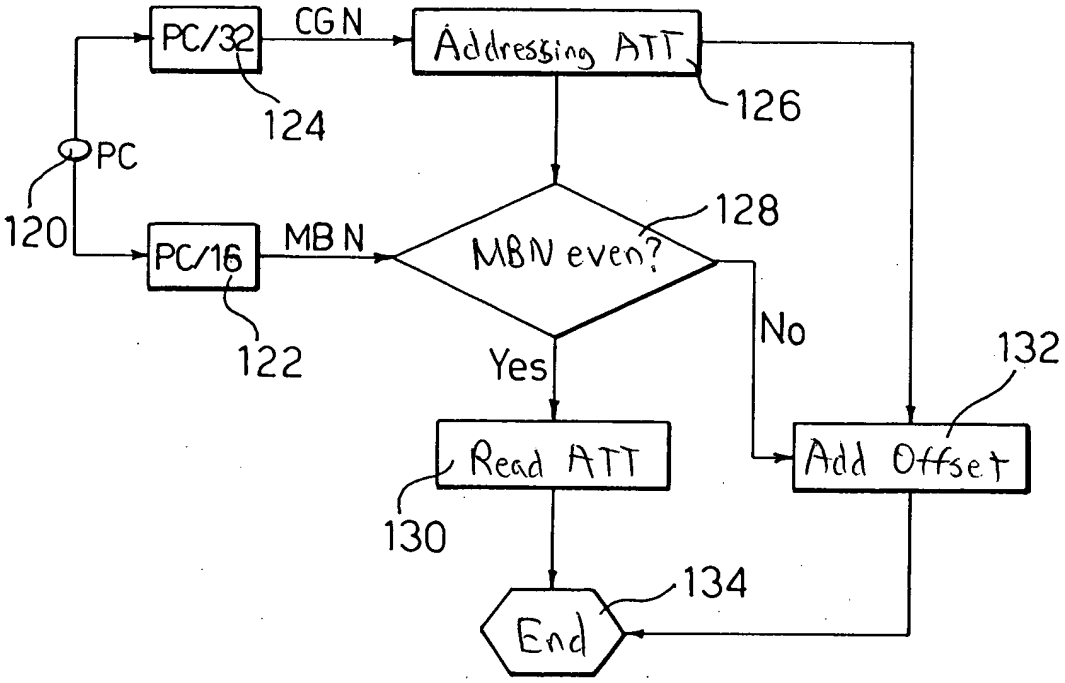
PC/32
CG N
Addressing ATT
PC
PC/16
MB N
MBN even?
Yes
No
Read ATT
Add Offset
End
120
122
124
126
128
130
132
134

Fig_12

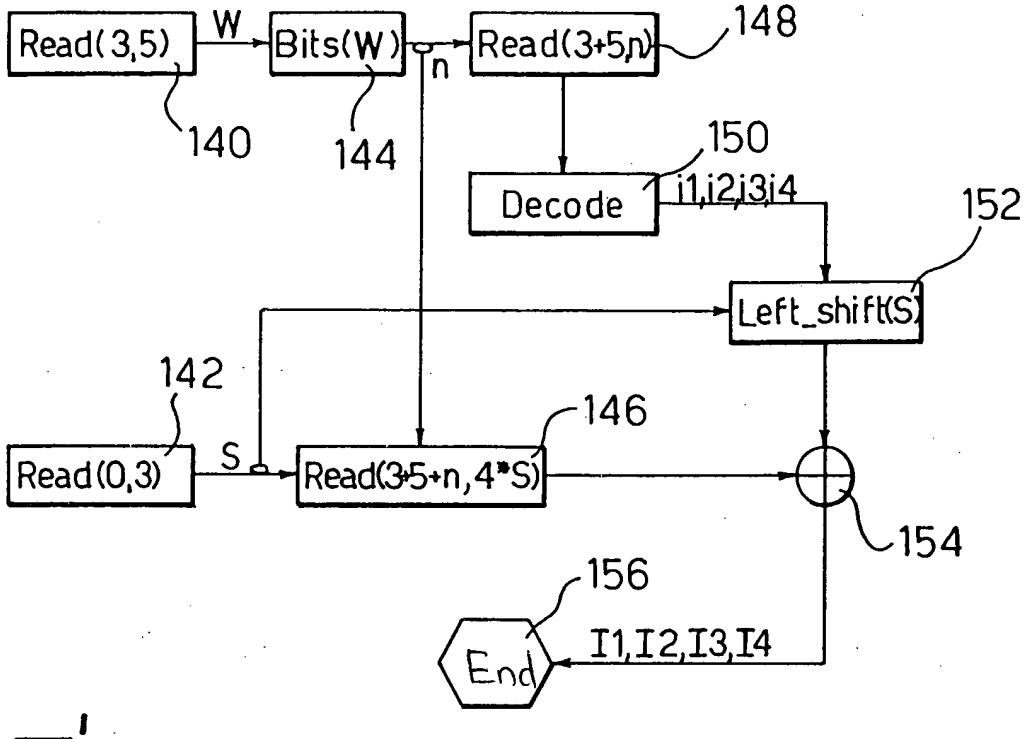
Read(3,5)
W
Bits(W)
n
Read(3+5,n)
148
140
144
150
Decode
i1,i2,i3,i4
152
Left_shift(S)
142
146
Read(0,3)
S
Read(3+5+n,4*S)
154
156
End
I1,I2,I3,I4

Fig_13

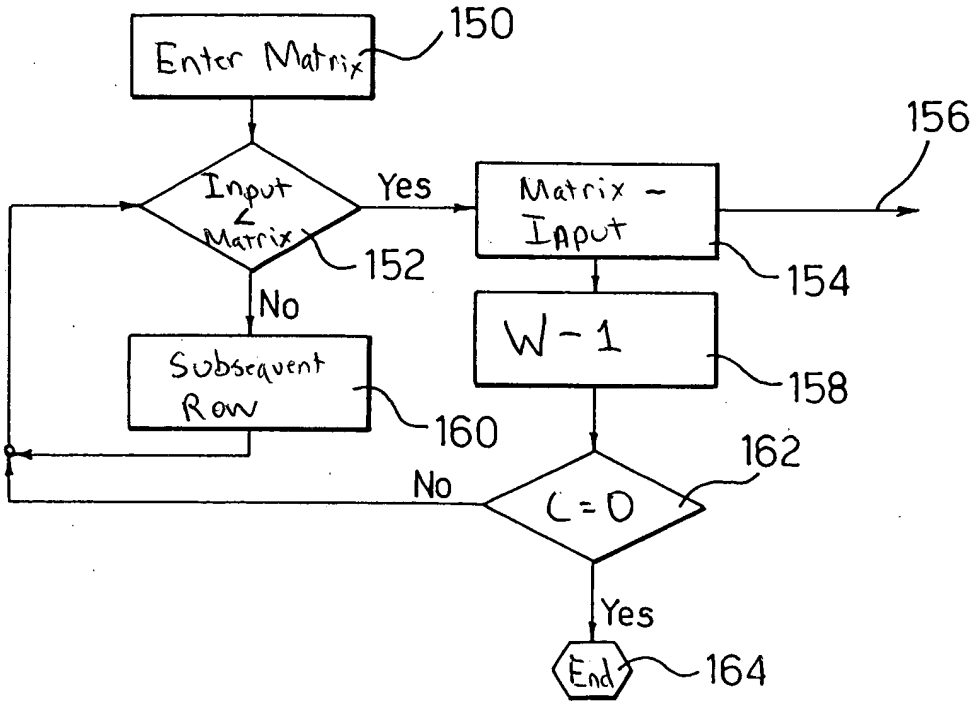
Enter Matrix
150
Input < Matrix
Yes
152
Matrix - Input
156
154
No
W - 1
158
Subsequent Row
160
162
No
C = 0
Yes
End
164

Fig_14

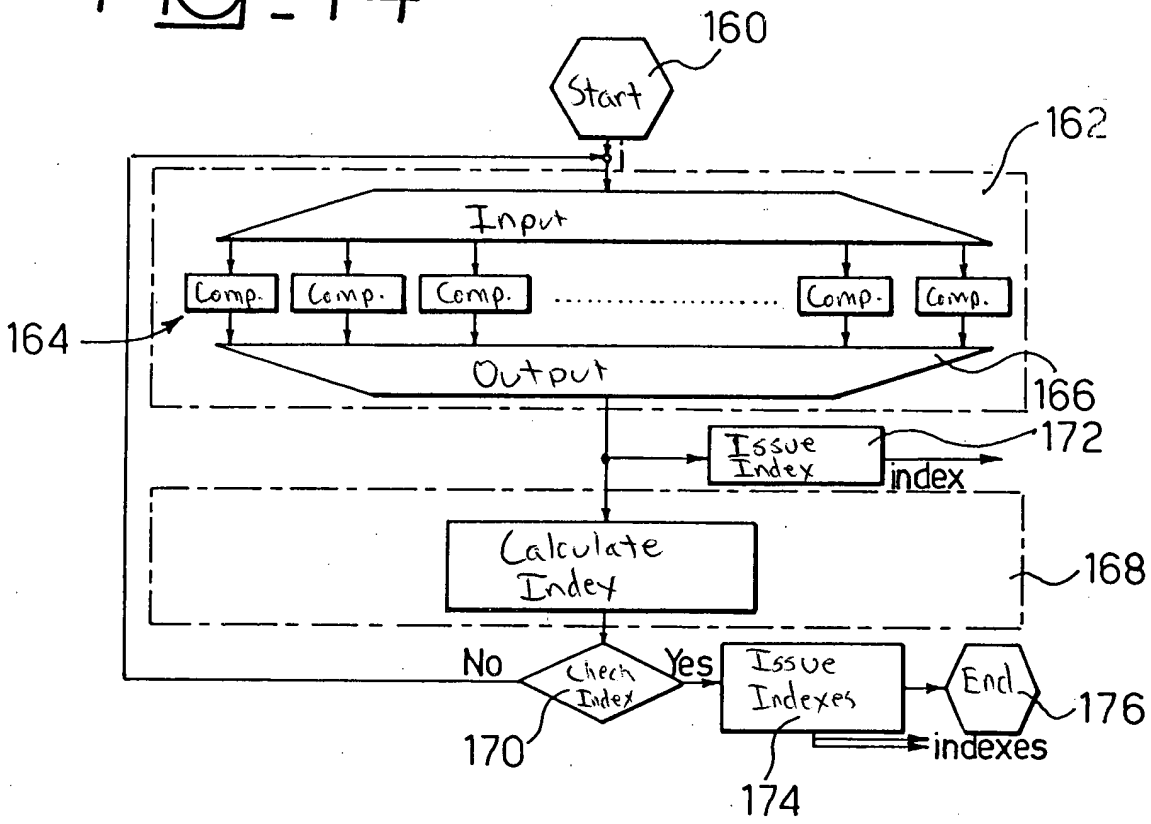
160
Start
162
Input
Comp.
Comp.
Comp.
Comp.
Comp.
164
Output
166
Issue Index
172
index
Calculate Index
168
No
Check Index
Yes
Issue Indexes
End
176
170
indexes
174

Fig_15

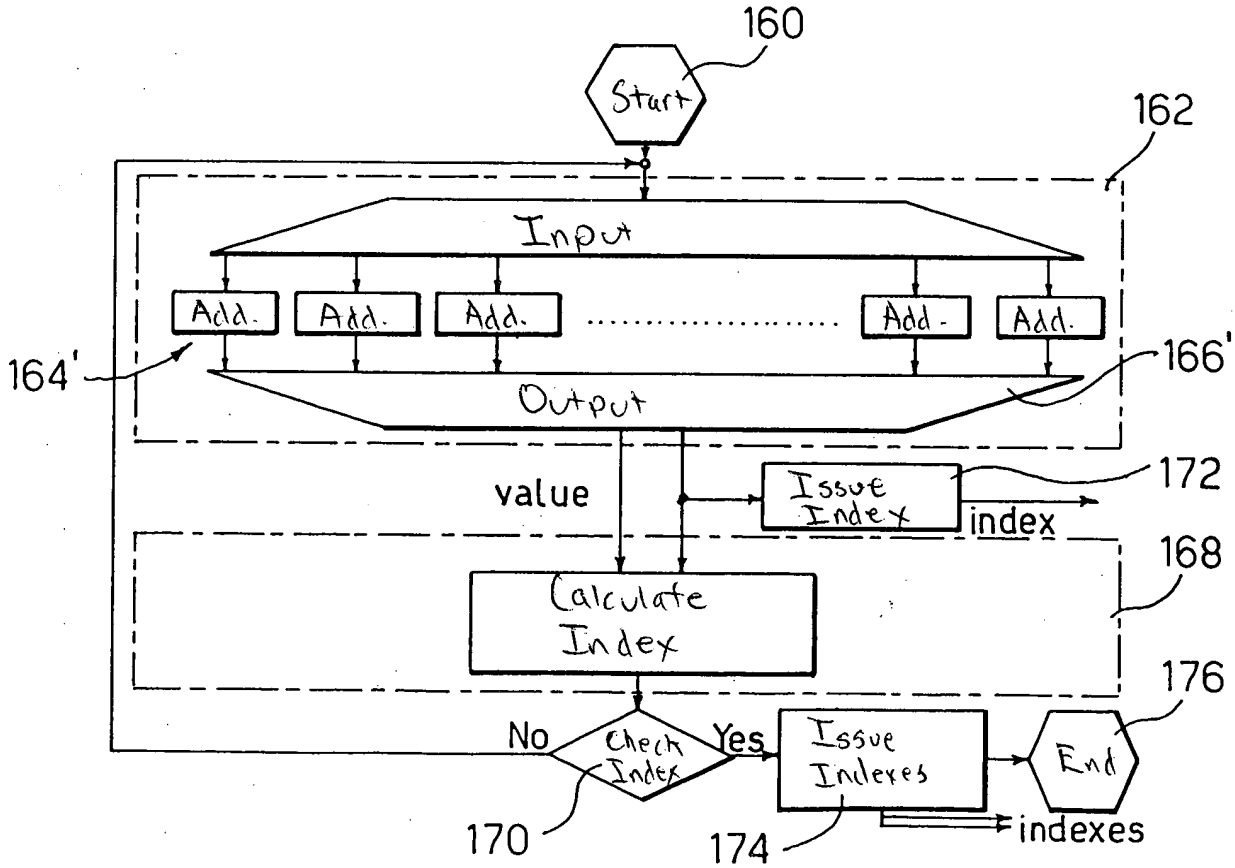
160
Start
162
Input
Add.
Add.
Add.
Add.
Add.
164'
166'
Output
value
Issue Index
172
index
168
Calculate Index
176
No
Check Index
Yes
Issue Indexes
End
170
174
indexes

Fig_16

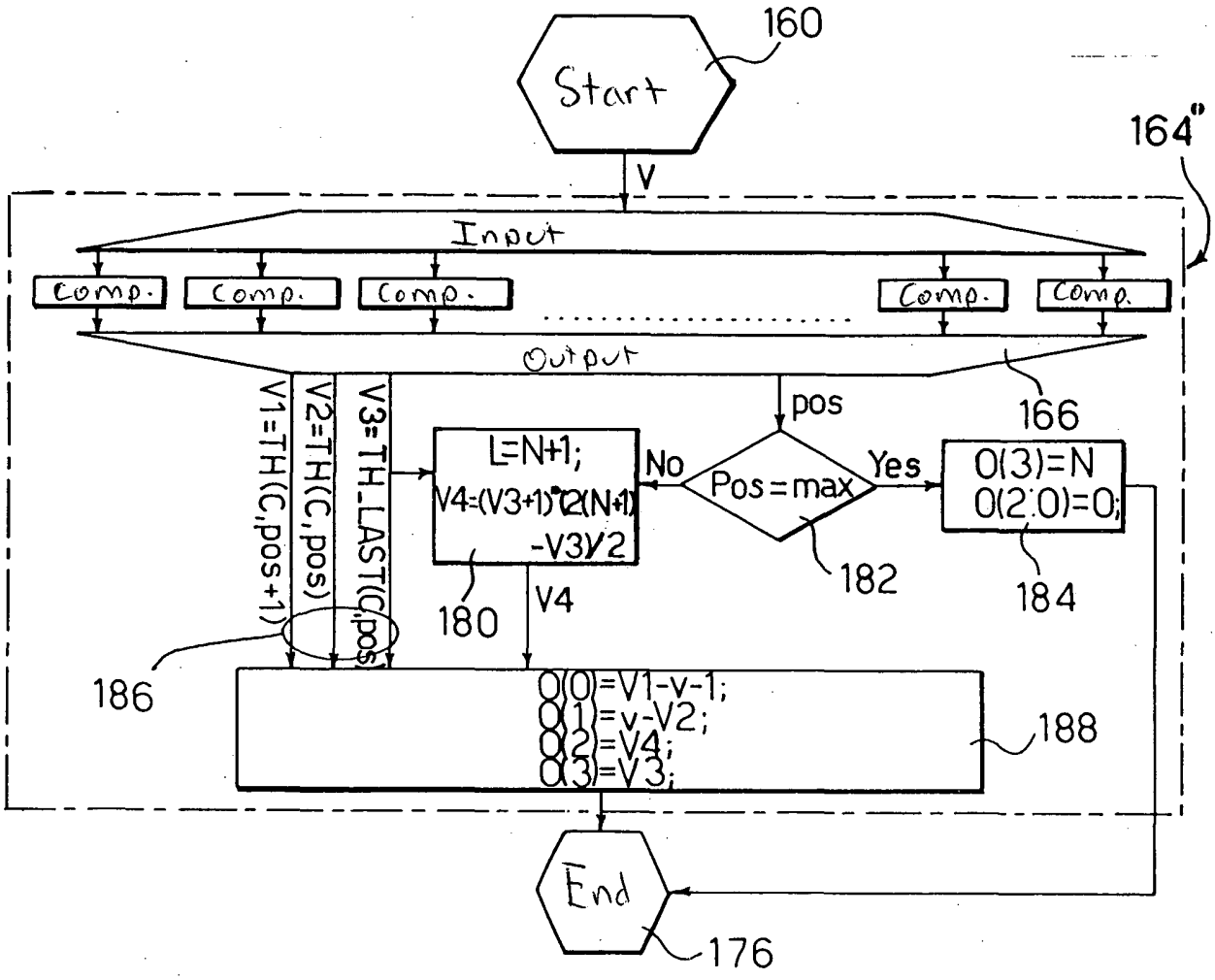
160
Start
164"
V
Input
Comp.
Comp.
Comp.
Comp.
Comp.
Output
166
V1=TH(C,pos+1)
V2=TH(C,pos)
V3=TH_LAST(C,pos)
pos
L=N+1;
V4=(V3+1)*2^(N+1)
-V3V2
No
Pos=max
Yes
O(3)=N
O(2:0)=0;
182
184
180
V4
186
O(0)=V1-v-1;
O(1)=v-V2;
O(2)=V4;
O(3)=V3;
188
End
176

Fig_17

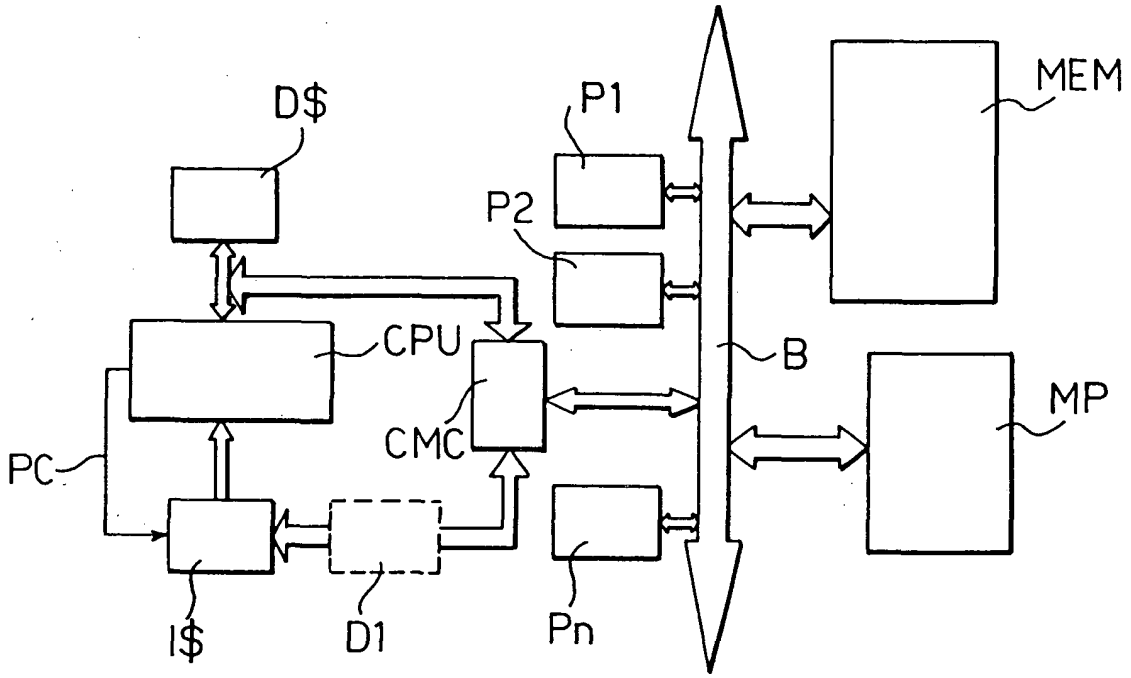
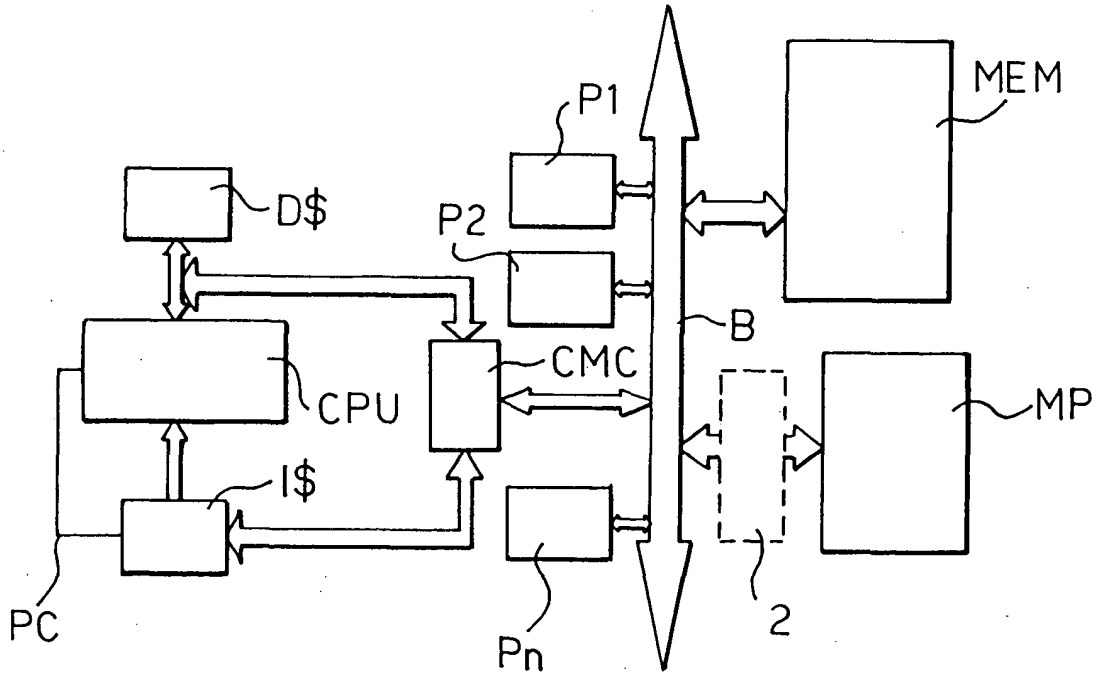
Fig_18